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Design and Implementation of a Low-Power, High-Speed Comparator

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Abstract

In the existing world, where demand for portable battery operated devices is increasing, a major push is given towards low power methodologies for high speed applications. Symmetric circuits with regenerative feedback give opportunity to identify new structures that may be particularly useful. Regenerative feedback is usually used in Dynamic Comparators and rarely in non-clocked comparators. Dynamic Comparators are generally used in the design of high-speed Analog to Digital Converters and can easily be designed. The existing comparator requires high accuracy timing Clkb, maximum drive current and high power. To overcome the disadvantages of the existing comparator a new dynamic comparator has been proposed in this paper that uses low power and has less delay. For the performance verification, the design is simulated in Cadence gpdk 180nm Technology at 1.8 Voltage Supply. Post Layout Simulation results in 180nm CMOS technology shows that power consumption is reduced by 58% and delay time is reduced by 41%.

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Keywords: Double-Tail Comparator; Dynamic Latch Comparator; Dynamic Clocked Comparator;

1. Introduction

The circuit which is used for converting analog signals to digital signals is the comparator which is one of the basic building blocks in most analog-to-digital converters (ADCs). Many applications, such as memory sending circuits and on chip transceivers etc. are widely using comparators. CMOS dynamic latched comparators using a set of back-to-back cross coupled inverters to convert a small input-voltage difference to a full scale digital level in a

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short duration is power efficient and better than carrying out multistage of linear application [2].

The charge-transfer preamplifier which does not need static power was proposed in [1]. A comparator has been proposed [3,4,6] using latch load to reduce power and offset voltage based on which a double-tail dynamic comparator was designed [5] with a set of input and cross-coupled stage.

In this paper, a comparator has been proposed which uses low power and operates faster when compared to the existing comparator and it is organized as follows. The operation of the dynamic comparators with its advantages and disadvantages is explained in Section 2 and the Proposed Comparator is discussed in Section 3. Results are addressed in Section 4 and followed by conclusions in Section 5.

2. Dynamic Comparators

Dynamic Comparators are also called as Clocked Comparators. Regenerative feedback is often used in dynamic comparators and occasionally in non-clocked comparators. Dynamic Comparators are mostly used in the design of high-speed ADCs.

2.1 Conventional Dynamic Comparator

The conventional dynamic comparator is shown in figure 1, which is widely used in analog and digital converters is explained as follows. When CLK=0, during the reset phase then the transistor M_{tail} will be off. The transistors M5 and M6 which are called reset transistors becomes on and makes both the output nodes 'Outp' and 'Outn' to turn into level V_{DD} for beginning of a start condition. When CLK becomes V_{DD} then the M5 and M6 transistors are off, and M_{tail} becomes on then the output voltages (Outp and Outn), which were at V_{DD} start to fall with different rates based on the corresponding discharging rates. Assume the case where the voltage V_{INP} is greater than V_{INN} then the voltage at Outp node discharges faster than the voltage at Outn node. As the voltage at Outp node which is discharged by M2 transistor drain current then the voltage goes down to $V_{DD}-|V_{thp}|$ before the voltage at Outn node which is discharged by M1 transistor drain current, accordingly M7 transistor becomes on. Thus, the back to back inverters start the latch generation and the voltage at Outn node becomes V_{DD} and the voltage level at Outp node falls down to ground.

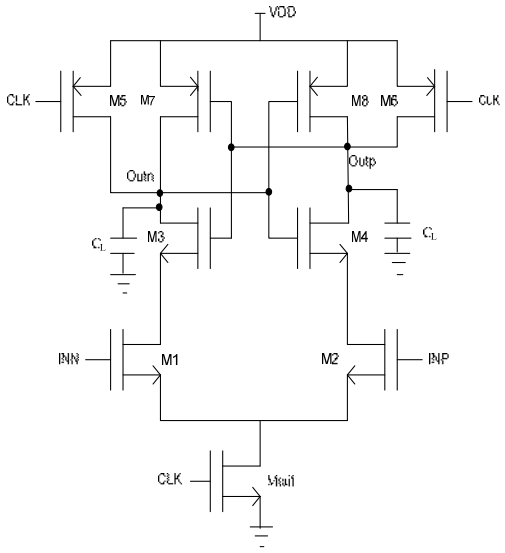

Fig 1: Schematic diagram of the Conventional Dynamic Comparator

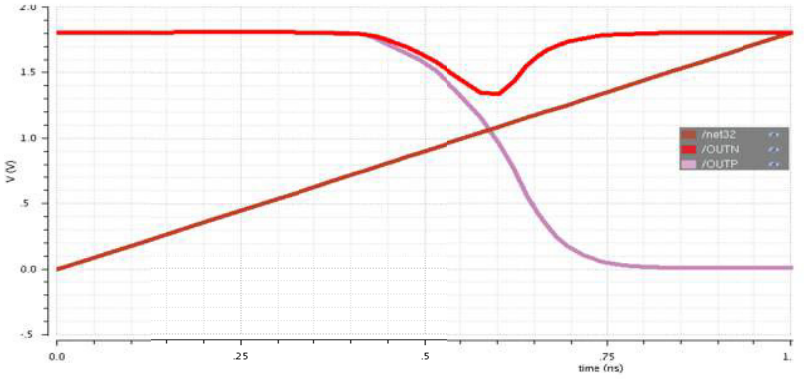

Fig 2: Simulation results of the Conventional Dynamic comparator

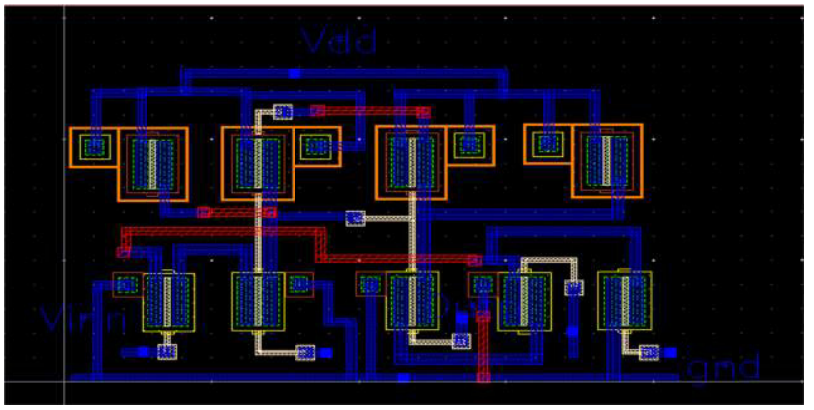

Fig 3: Layout of the Conventional Dynamic Comparator

If V_{INN} voltage is greater than V_{INP}, the circuit works vice versa. The capacitive discharge of C_L (Load Capacitance) until the M7 and M8 transistors turns on represents the delay. If the voltage at node INP is bigger than INN (i.e $V_{INP}>V_{INN}$), then the M2 transistor drain current causes faster discharge of 'Outp' node when compared to 'Outn' node which is being by transistor M1 with little current. Simulation results show an increase in the total delay.

This comparator works at high input impedance and has good robustness against noise and mismatch [2]. But, a high supply voltage is necessary to drive the several stacked transistors for less delay time. At the starting point of making decision, M3 and M4 transistors leads the positive feedback to make the voltage level of one output node to be dropped to a smaller level so as to make the M5 and M6 transistors for complete regeneration. But, the delay duration becomes large due to lower transconductance. Another disadvantage is that the current flows through the transistor M_{tail1}which supplies to differential amplifier and also to the cross coupled inverters.

2.2 Conventional Double-Tail Comparator

The circuit diagram of Conventional Double-tail Comparator is shown in figure 4. This comparator has less stacking and can run at lower supply voltages. It also enables a large current to flow through the back to back inverters for fast latching even if a small current flows though the transistor M_{tail1} in the input stage.

This comparator operates as follows. When CLK=0 then the transistors M_{tail1}, and M_{tail2} becomes off and M3-M4 transistors raises the voltage at fn and fp nodes to V_{DD} and the transistors M_{R1} and M_{R2} discharge the Outn and Outp nodes to ground. During decision-making phase i.e when CLK=V_{DD}, then the transistors M_{tail1} and M_{tail2} becomes on and the transistors M3-M4 becomes off and the voltages at nodes fn and fp decline with the rate defined by $IM_{tail1}/C_{fn(p)}$ and an input-dependent differential voltage $V_{fn(p)}$ will start. The intermediate stage which is being formed by the transistors M_{R1} and M_{R2} passes Vfn(p) to the cross coupled inverters and a good shielding is being generated between the input and output which reduces the kickback noise. In comparison to the conventional dynamic comparator the delay has been reduced. But in this comparator, both $M_{R1}$and M_{R2} transistors are in finally cut-off as the voltages at both fp and fn nodes reduces to ground, since they don't improve the transconductance of the latch.

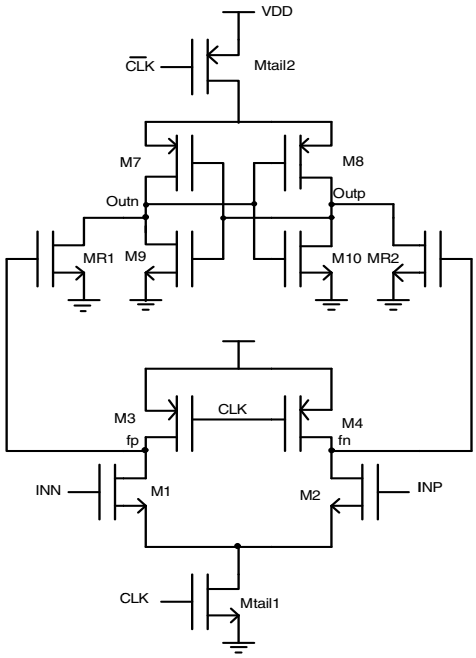

Fig 4: Schematic diagram of the Conventional Double-Tail Comparator

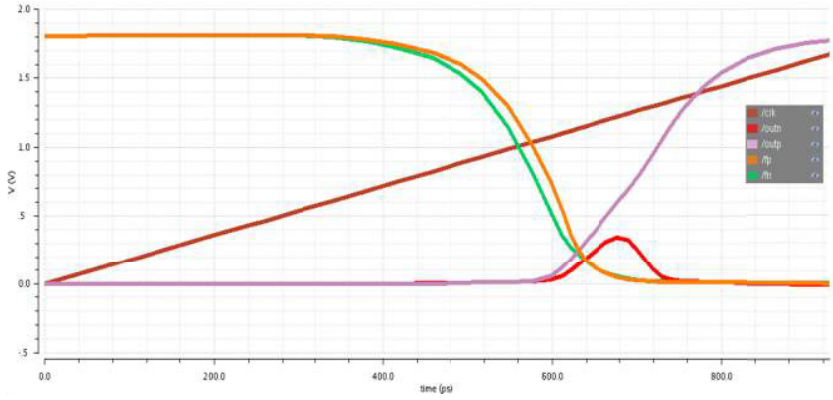

Fig 5: Simulation Results of the Conventional Double-Tail Comparator

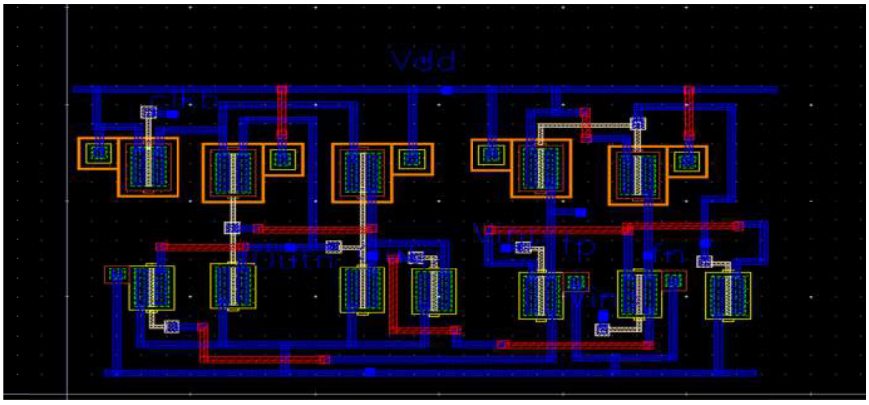

Fig 6: Layout of Conventional Double-Tail Comparator

This comparator operates as follows. When CLK=0 then the transistors M_{tail1}, and M_{tail2} becomes off and M3-M4 transistors raises the voltage at fn and fp nodes to V_{DD} and the transistors M_{R1} and M_{R2} discharge the Outn and Outp nodes to ground. During decision-making phase i.e when CLK=V_{DD}, then the transistors M_{tail1} and M_{tail2} becomes on and the transistors M3-M4 becomes off and the voltages at nodes fn and fp decline with the rate defined by $IM_{tail1}/C_{fn(p)}$ and an input-dependent differential voltage $V_{fn(p)}$ will start. The intermediate stage which is being formed by the transistors M_{R1} and M_{R2} passes Vfn(p) to the cross coupled inverters and a good shielding is being generated between the input and output which reduces the kickback noise. In comparison to the conventional dynamic comparator the delay has been reduced. But in this comparator, both $M_{R1}$and M_{R2} transistors are in finally cut-off as the voltages at both fp and fn nodes reduces to ground, since they don't improve the transconductance of the latch.

2.3. Existing Dynamic Comparator

Figure 7 shows the schematic diagram of the existing dynamic comparator [6]. The latch regeneration speed of this comparator has been increased when compared to the previous comparator. Accordingly, two control transistors M_{C1} and M_{C2} are added together to the first stage in parallel to the M3/M4 transistors in a cross coupled manner.

The operation is explained as follows. When CLK=0 then the transistors M_{tail1} and M_{tail2} becomes off and the transistors M3 and M4 makes the voltage of both the fn and fp nodes to reach V_{DD}, by avoiding static power dissipation hence transistors M_{C1} and M_{C2} falls to cut-off. M_{R1} and M_{R2} transistors restart both latch outputs to ground. When CLK=V_{DD} then the transistors M_{tail1} and M_{tail2} becomes on and the transistors M3 and M4 switches off. At the initial stage of this phase, the control transistors still act to be off as both the nodes fn and fp are at the level V_{DD}. Therefore, the voltages at fn and fp nodes begin to fall down with different rates according to the input voltages. If the voltage V_{INP} is greater than V_{INN}, thus fn drops rapidly than fp (since M2 contributes more current than M1).

As long as the voltage drops at fn node, the control transistor M_{C1} begins to start, making the voltage at fp node to raise its level and the other control transistor M_{C2} still is in off state making the voltage at fn node to be dropped. In conventional double-tail comparator, ΔVfn/fp is just a function of input transistor transconductance and input voltage difference in this structure as soon as the comparator detects that for instance mode fn discharges faster and pMOS transistor (M_{C1}) turns on, making the node fp to raise its level. Therefore, by time passing, the difference between fn and fp ($\Delta V_{fn/fp}$) increases in an exponential manner, leading to the regeneration time. To overcome the static power consumption, two nMOS transistors M_{sw1} and M_{sw2} are used below the input transistors.

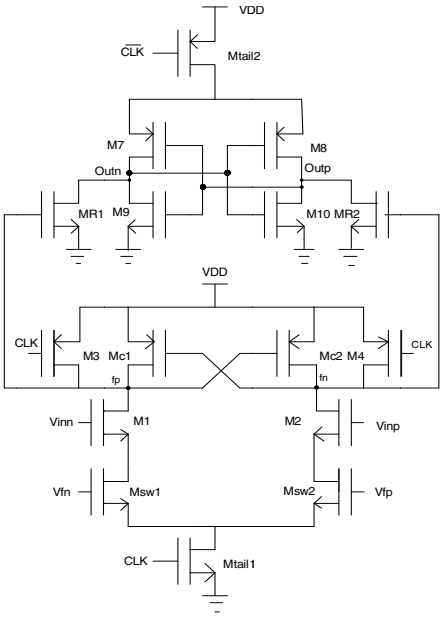

Fig 7: Schematic diagram of the existing dynamic comparator

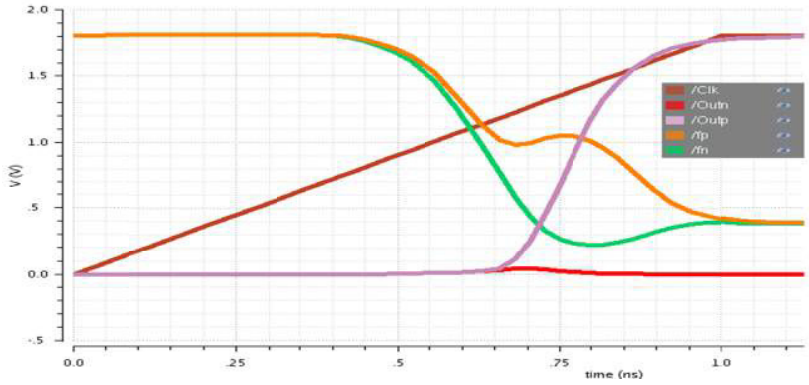

Fig 8: Simulation Results of the Existing Dynamic Comparator

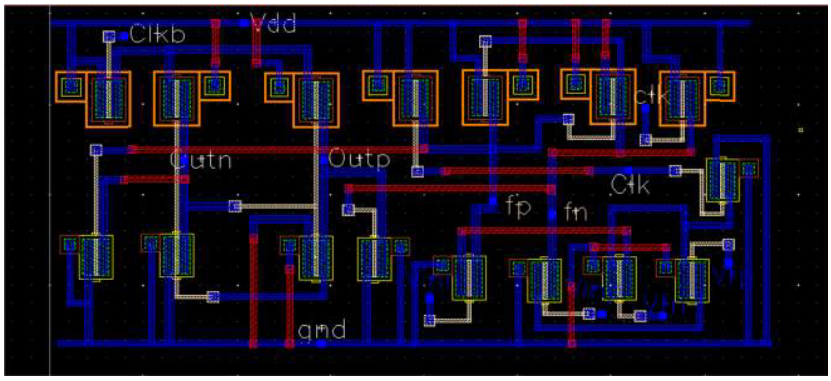

Fig 9: Layout of the Existing Dynamic Comparator

3. Proposed Comparator

The schematic diagram of the proposed comparator is shown in the figure 10 below. The main aim of the proposed comparator is to decrease the power consumption, delay and to increase the latch regeneration speed compared to the existing dynamic comparator [5].The operation is explained as follows. When CLK=0, then the transistor M13 becomes off and the transistors M9 and M12 makes the output nodes 'fn' and 'fp' to reach to V_{DD}, thus the transistors M_{C1} and M_{C2} are in cut-off. After the reset phase i.e during decision making phase, the transistors M_{C1} and M_{C2} are in off stage itself and both the output nodes 'fn' and 'fp' which are at V_{DD} start to fall with distinct rates according to the given input voltages. If the voltage of V_{INP} is greater than V_{INN}, then 'fp' drops faster than 'fn', because M2 draws more current than M1.

During the time, when the voltage at 'fp' starts decreasing then the correspondent transistor M_{C1} turns to on stage, making the 'fn' node to increase its level. Hence, the other transistor M_{C2} continues to be disconnected, by providing 'fp' to be discharged. When the comparator finds that 'fp' is discharging quickly, then the pMOS transistor M_{C1} increases the level of 'fn'. At the starting point of the decision making phase, both the 'fp' and 'fn' nodes had been setup to V_{DD} but later on start to discharge with different rates to control the current to be drawn from V_{DD}. To overcome the high accuracy timing Clkb in the existing comparator M1 and M2 are used instead of M_{tail2}.

The sensitivity of the comparator enhances the gain of latch of the second stage and the clock-driving necessity is not required as the comparator works in one-phase clock. The offset has also been decreased because the gain output is taken form the second input- transistors (M1/M2 and M5/M6) and the drive current is decreased to half of the tail current comparing with the previous comparator as it was divided into M1 and M2 transistors.

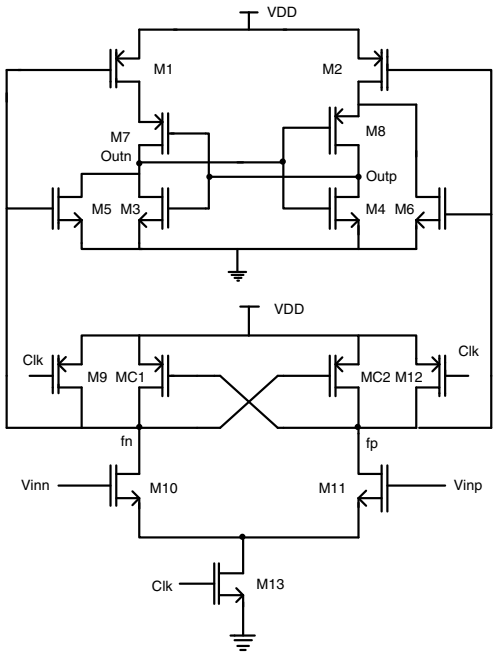

Fig 10: Schematic diagram of the Proposed Comparator

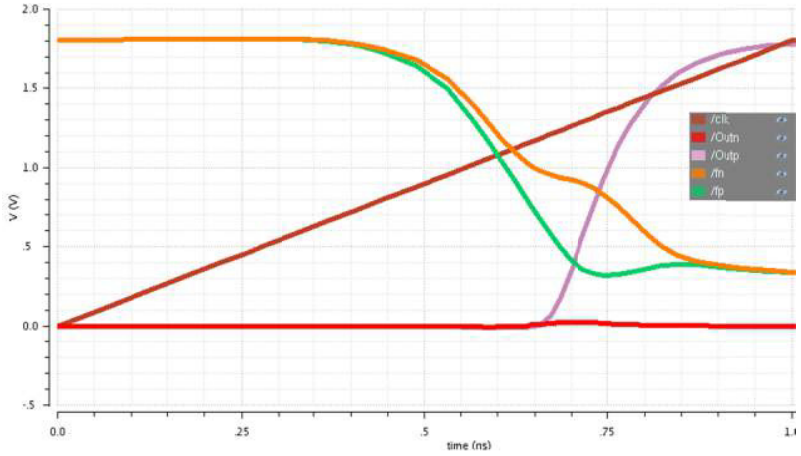

Fig 11: Simulation Results of the Proposed Comparator

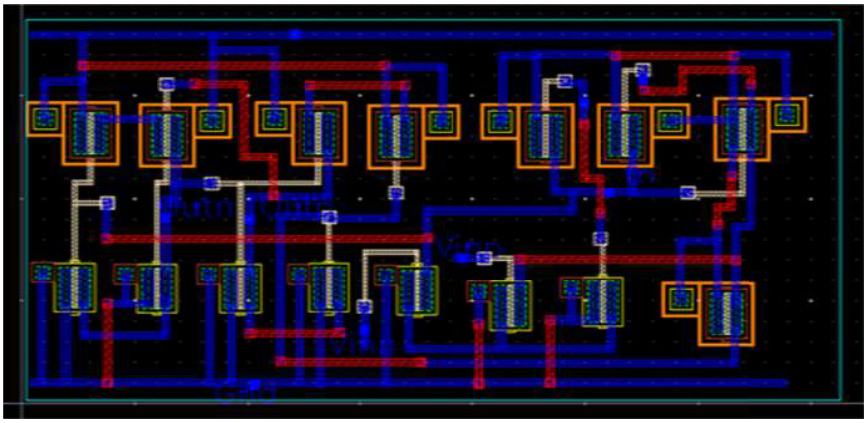

Fig 12: Layout Results of the Proposed Comparator

Table 1: Performance comparisons of different comparators

Comparator Structure	Conventional Dynamic comparator	Double-tail Dynamic Comparator	Existing Dynamic Comparator	Proposed Comparator
Technology CMOS	180nm	180nm	180nm	180nm
Supply voltage (V)	1.8V	1.8V	1.8V	1.8V
Delay/log (ps/dec)	285	120	113.5	66.56
Power (µw)	436.3	337.5	581.3	242.6
Layout Area	16 µ x 16 µ	28 µ x 12 µ	38 µ x 18 µ	33 µ x 16 µ

4. Results

In order to compare the proposed comparator with the conventional, double-tail dynamic and exiting comparator, all circuits have been designed and implemented in 180 nm CMOS technology with V_{DD}=1.8V using Cadence Virtuoso tools. The Proposed Comparator designed uses low power, less delay and area efficient when compared to previously designed comparators.

5. Conclusion

This project has been simulated using Cadence Virtuoso tool. The proposed comparator operates faster and can be used in lower supply voltages. The Proposed Comparator reduces the power from 581.3 μw to 242.6 μw which is approximately 58% and delay has been reduced from 113.5ps to 66.56ps which is approximately 41%.

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